A7 cont'd

then, reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner.

REMARKS:

The amendment to page 1 of the specification updates the citation of the parent application. The amendment to page 6 of the specification eliminates redundant text.

Claims 1-12 stand rejected under 35 U.S.C. 103(a), as being unpatentable over U.S. Patent 6,087,227 (Hsu) in view of U.S. Patent 6,197,646 (Goto). In response, Applicant respectfully contends that these claims as amended and new claim 13 are patentable over the cited art for the flowing reasons.

Support for the limitation added to the last paragraph (following "wherein") of each of amended claims 1 and 8, and for the new claim, can be found in the specification, for example, at page 5, lines 3-16, the paragraph spanning pages 5 and 6, and the paragraph spanning pages 9 and 10. The specification explains that the "predetermined property" of the metal deposited in step (b) of claim 1 or 8 can be a predetermined thickness of the deposited metal.

Hsu fails to teach or suggest controlling a parameter of deposition of cobalt layer 430 (or any other metal deposition parameter) such that cobalt layer 430 (or another deposited metal layer) has a predetermined property that limits metal (e.g., cobalt) salicide crawl during subsequent formation of a metal salicide region by reacting metal in layer 430 (or other metal layer) with silicon in an exposed silicon surface, as recited in amended claims 1 and 8. The Examiner has not contended that Hsu includes such a teaching or suggestion.

Goto teaches (with reference to Fig. 6A) that the thickness of a deposited metal layer affects the sheet resistance of metal salicide produced by subjecting the metal layer to an annealing step. However, Goto does not teach or suggest forming a photoresist masking layer on MOS transistor structures where metal salicide regions are to be formed, then removing portions of a metal layer (and any capping layer thereon) from portions of the structures where metal salicide exclusion regions are to be formed, then stripping the masking layer, and then reacting metal in the remaining portions of the metal layer with silicon in exposed silicon surfaces to form metal salicide regions. Rather, Goto teaches (with reference to Figs. 1A-1F) a very different, conventional metal salicide region formation method that does not include a metal removal step prior to metal salicide region formation.

As explained in the specification, the claimed method can achieve the unexpected benefit of reducing salicide crawl over and under metal salicide exclusion regions (e.g., gate sidewall spacers) adjacent to a metal salicide region. Since metal is removed from locations where metal salicide exclusion regions are to be formed, there is only a limited amount of metal (i.e., the metal that remains after the removal step) available to form metal salicide regions in accordance with the invention. By controlling the thickness of the metal that remains after the removal step (by controlling the pre-removal step of depositing the metal), the metal salicide formation reaction is controlled and can be driven to completion (in the sense that the completion occurs when the limited amount of available metal is consumed by the reaction). The inventive salicide-forming reaction can thus be "source limited" in the sense that it is limited by the amount of metal available for reaction.

In contrast, when performing Goto's conventional metal salicide formation method, there is an effectively unlimited supply of metal available for forming salicide. There is no teaching or suggestion determinable from Goto that a limited amount of metal (i.e., metal remaining after a removal step) should be made available to form metal salicide regions, and that such limited

amount of metal should have its thickness (or another of its parameters) controlled during deposition to control a metal salicide formation reaction (e.g., to drive the reaction to completion). Controlling the thickness of the metal layer deposited during Goto's method would apparently not limit the supply of metal available for forming salicide in accordance with Goto's method, and thus would not reduce salicide crawl as recited in amended claims 1 and 8.

There is no teaching determinable from Goto (or other art of record) that Hsu's method should be modified to reach the invention of amended claim 1 or 8.

Furthermore, neither Hsu nor Goto teaches or suggests a method including the steps of "depositing a metal layer having a predetermined thickness" over an IC structure, then removing portions of the metal layer, and then reacting nonremoved portions of the metal layer with silicon (of MOS transistor structures) to form metal salicide regions "in a source limited manner" as recited in new claim 13. As explained in the specification, metal salicide region formation is "source limited" when it is limited by the amount of metal available for reaction.

Thus, Applicant respectfully contends that claims 1, 8, and 13 (and all claims depending therefrom) are patentable over Hsu and Goto, whether these references are considered individually or in combination.

Respectfully submitted,
GIRARD & EQUITZ LLP

Dated: 11/11/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. NSC1-G0610 [P04402 P01]

APPENDIX

The section entitled "Cross-Reference to Related Application" on page 1 is amended as follows:

This application is a continuation-in-part of U.S. Application No. 09/430,348, filed on October 29, 1999, and issued as U.S. Patent 6,329,287 [now pending].

Page 6, lines 5-9 are amended as follows:

[then, removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;]

then, removing the metal layer (as well as the capping layer, if any) from those MOS transistor structures where metal salicide exclusion regions are to be formed;

Claims 1-3, 5, 8-10, and 12 are amended as follows:

1. (Amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on portions of the [those] MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property, and the at least one predetermined property [is such that] limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed [in step (f) has at least one predetermined attribute].

2. (Amended) The method of claim 1, wherein said at least one predetermined [attribute of said] property is such that at least one of the metal salicide regions [is]has a predetermined sheet resistance.

3. (Amended) The method of claim 1, wherein said at least one predetermined [attribute of said] property is such that at least one of the metal salicide regions [is]has a predetermined conductivity.

5. (Amended) The method of claim 1, wherein the removal during step (d) of the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and step (b), are [is] performed in a manner significantly limiting metal salicide crawl during step (f) over and under at least one of the portions of the MOS structures where metal salicide regions are to be[the metal salicide regions] formed[during step (f)].

8. (Amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on portions of the [those] MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property, and the at least one predetermined property [is such that] limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed [in step (g) has at least one predetermined attribute].

9. (Amended) The method of claim 8, wherein said at least one predetermined [attribute of said] property is such that at least one of the cobalt salicide regions [is]has a predetermined sheet resistance.

10. (Amended) The method of claim 8, wherein said at least one predetermined [attribute of said] property is such that at least one of the cobalt salicide regions [is]has a predetermined conductivity.

12. (Amended) The method of claim 8, wherein the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, and step (b), are [is] performed in a manner significantly limiting cobalt salicide crawl during step (g) over and under at least one of the portions of the MOS structures where cobalt salicide regions are to be[the cobalt salicide regions] formed[during step (g)].